CLAIMS

I CLAIM:

1. A semiconductor system comprising a semiconductor device in a semiconductor region of a substrate characterized by at least one selection from the group consisting of:

> said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and
>
> said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels;

said semiconductor device comprising at least one junction(s) characterized by at least one selection from the group consisting of:

> P-N rectifying;
>
> Schottky barrier rectifying; and
>
> formed from non-semiconductor, and semiconductor, components, wherein said non-semiconductor component of said at least one junction(s) is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced.

2. A semiconductor system comprising a semiconductor device in a semiconductor region of a substrate characterized by at least one selection from the group consisting of:

said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and

said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels;

said semiconductor device comprising a plurality of junctions, each being characterized by a selection from the group consisting of:

P-N rectifying;

Schottky barrier rectifying; and

formed from non-semiconductor, and semiconductor, components, wherein said non-semiconductor component of said at least one junction(s) is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced; and

arranged as a selection from the group consisting of a - g:

a.

being essentially ohmic; and

comprising non-semiconductor, and semiconductor, components, wherein said non-semiconductor component is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced;

b.

comprising non-semiconductor, and semiconductor, components, wherein said non-semiconductor component is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced; and

comprising non-semiconductor, and semiconductor, components, wherein said non-semiconductor component is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced;

c.

being essentially ohmic;

comprising non-semiconductor, and semiconductor, components, wherein said non-semiconductor component is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced;

comprising non-semiconductor, and semiconductor, components, wherein said non-semiconductor component is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced; and

being essentially ohmic;

d.

being substantially ohmic;

being rectifying;

being rectifying; and

being substantially ohmic;

e.

being rectifying; and

being rectifying;

f.

being substantially ohmic; and

being rectifying;

g.

comprising non-semiconductor, and semiconductor, components, wherein said non-semiconductor component is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced;

being essentially ohmic;

being essentially ohmic; and

comprising non-semiconductor, and semiconductor, components, wherein said non-semiconductor component is comprised of at least one material(s) which forms rectifying junctions with both N and P-type semiconductor, whether said semiconductor type is metallurgically or field induced;

3. Inverting and non-inverting devices with operating characteristics similar to dual device seriesed N and P-Channel MOSFETS CMOS systems; comprising in use, two oppositely facing electrically interconnected rectifying diodes in a semiconductor region of a substrate characterized by at least one selection from the group consisting of:

said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and

said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially

different doping levels;

wherein a forward direction of rectification of each of said electrically interconnected rectifying diodes changes depending upon what doping type, (N or P), be it metallurgically or field induced, is present in the semiconductor, said inverting and non-inverting single device equivalents to dual device seriesed N and P-Channel MOSFETS CMOS systems further comprising gate means for field inducing effective doping type in said semiconductor, said gate means being set off from said semiconductor by insulator and each of said electrically interconnected rectifying diodes having an electrically non-interconnected terminal; and wherein, in use, different voltages are applied to the non-electrically interconnected terminal of each of the oppositely facing rectifying diodes, and a voltage between said applied different voltages, inclusive, is monitored at the electrical interconnection between said two oppositely facing rectifying diodes, which monitored voltage responds as a function of applied gate voltage, said monitored voltage being essentially electrically isolated from said gate voltage and appearing at said electrical interconnection between said two oppositely facing rectifying diodes primarily through the rectifying diode which becomes forward biased;

the basis of operation of said gate voltage channel induced semiconductor devices being that said rectifying junctions are comprised of material(s) that form a rectifying junction to semiconductor when it is doped either N or P-type by either metallurgical or field induced means.

4. A semiconductor device formed in a semiconductor region characterized as single crystal or amorphous or an intermediate thereto, in which are essentially homogeneously simultaneously present both N and P-type metallurgical dopants, said

semiconductor device comprising at least one rectifying junction which is formed from non-semiconductor and semiconductor components, wherein said junction non-semiconductor component is comprised of material(s) which, in use, form a rectifying junction with both N and P-type semiconductor, whether metallurgically or field induced.

5. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems, said inverting gate voltage channel induced semiconductor device being formed in a semiconductor epi-layer or substrate characterized by a selection from the group consisting of:

> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and
>
> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels;

said inverting gate voltage channel induced semiconductor device comprising two junctions, termed source and drain, which are separated by a first semiconductor channel region, and further comprising two additional junctions, termed source and drain, which are separated by a second semiconductor channel region, wherein gates, to which semiconductor channel region field induced effective doping effecting voltage can be applied, are associated with each of the first and second semiconductor channel regions, said gates being offset from said first and second semiconductor channel regions by insulating material; such

that during use application a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will attract holes to said first and second semiconductor channel regions, the purpose of applying such gate voltage being to affect field induced effective doping type of said first and second semiconductor channel regions between respective source and drain junctions, which source junctions are each essentially non-rectifying, and which drain junctions are rectifying junctions;

in which inverting gate voltage channel induced semiconductor device the rectifying drain junction associated with said first semiconductor channel region is electrically interconnected with the rectifying drain junction associated with said second semiconductor channel region, and in which said gates associated with said first and second channel regions are electrically interconnected;

such that during operation the electrically noninterconnncted essentially non-rectifying source junctions are held at different voltages, and application of a gate voltage affects semiconductor channel region effective doping type in both said first and second channel regions by field induced means, and thus which electrically interconnected rectifying drain junction forward conducts as a result of semiconductor type metallurgically present or field induced by said applied gate voltage, thereby controlling the voltage present at the electrically interconnected rectifying drain junctions essentially through said forward conducting rectifying drain junction;

the basis of operation of said inverting gate voltage channel induced semiconductor device being that said rectifying drain

junctions associated with said first and second semiconductor channel regions thereof are comprised of at least one material that forms a rectifying junction to a semiconductor channel region when it is either N or P-type by either metallurigical or field induced means, and the presence of at least partially compensated semiconductor which comprises both N and P-type carriers enables easy provision of N and P-type channel region forming carriers via gate voltage application effected field effect means.

6. An inverting gate voltage channel induced semiconductor device as in Claim 5, in which the semiconductor further comprises at least one region of parasitic current flow blocking material which prevents parasitic currents from flowing to or away therefrom through said at least one region of parasitic current flow blocking material, said at least one region of parasitic current flow blocking material being present at at least one selection from the group consisting of:

physically a part of the inverting gate voltage channel induced semiconductor device and comprising an extention of the electrical interconnection between the rectifying drain junction associated with said first semiconductor channel region and the rectifying drain junction associated with said second semiconductor channel region; and

physically separate from the inverting gate voltage channel induced semiconductor device;

said at least one region of parasitic current flow blocking material forming rectifying junctions with both N and P-type metallurgical or field induced semiconductor.

7. An inverting gate voltage channel induced semiconductor device

with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems, said inverting gate voltage channel induced semiconductor device being formed in a compensated semiconductor epi-layer or substrate characterized by a selection from the group consisting of:

> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and
>
> said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels;

said inverting gate voltage channel induced semiconductor device comprising two junctions, termed source and drain, which are separated by a first semiconductor channel region, and further comprising two additional junctions, termed source and drain, which are separated by a second semiconductor channel region, wherein gates, to which semiconductor channel region effecting voltage can be applied, are associated with each of the first and second semiconductor channel regions, said gates being offset from said first and second semiconductor channel regions by insulating material;

such that during use application of a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will attract holes to said first and second semiconductor channel regions, the purpose of applying such gate voltage being to affect field induced

effective doping of said first and second semiconductor channel regions between respective source and drain junctions, which source junctions are each essentially non-rectifying when sufficient field induced effective doping is present in the channel region adjacent thereto, and which drain junctions are each rectifying when sufficient field induced effective doping is present in the channel region adjacent thereto;

in which inverting gate voltage channel induced semiconductor device the drain junction associated with said first semiconductor channel region is electrically interconnected with the drain junction associated with said second semiconductor channel region, and in which said gates associated with said first and second channel regions are electrically interconnected;

such that during operation the electrically noninterconnected source junctions are held at different voltages, and application of a gate voltage affects semiconductor channel region effective doping in said first and second channel regions by field induced means, and thus which electrically interconnected rectifying drain junction in said semiconductor forms, as a result of semiconductor type field induced by said applied gate voltage, and forward conducts, thereby controlling the voltage present at the electrically interconnected drain junctions essentially through said formed forward conducting rectifying drain junction;

the basis of operation being that the drain junctions associated with said first and second semiconductor channel regions are comprised of at least one material that forms a rectifying junction to a semiconductor channel region when it is caused to be either N or P-type by field induced means, and the presence of at least partially compensated semiconductor which comprises both N and P-type carriers enables easy provision of N and P-type channel region forming carriers via gate voltage application

effected field effect means.

8. An inverting gate voltage channel induced semiconductor device as in Claim 7, in which the semiconductor further comprises at least one region of parasitic current flow blocking material which prevents parasitic currents from flowing to or away therefrom through said at least one region of parasitic current flow blocking material, said at least one region of parasitic current flow blocking material being present at at least one selection from the group consisting of:

physically a part of the inverting gate voltage channel induced semiconductor device and comprising an extention of the electrical interconnection between the rectifying drain junction associated with said first semiconductor channel region and the rectifying drain junction associated with said second semiconductor channel region; and

physically separate from the inverting gate voltage channel induced semiconductor device;

said at least one region of parasitic current flow blocking material forming rectifying junctions with both N and P-type metallurgical or field induced semiconductor.

9. An inverting gate voltage channel induced semiconductor device in Claim 7 in which the semiconductor channel region and, when formed, adjacent drain junction which is not forward conducting, is characterized by at least one selection from the group consisting of:

a. being functionally comprised of two regions across which voltage can drop, namely an onset of pinch-off region and a channel region;

b. being functionally comprised of three regions across which voltage can drop, namely an onset of pinch-off region, a portion of the channel region which is populated with some gate voltage field induced carriers, and a formed reverse biased rectifying junction.

10. An inverting gate voltage channel induced semiconductor device as in Claim 7, in which the semiconductor channel region and adjacent formed rectifying drain junction which is forward conducting is characterized as comprising a field induced carrier containing channel region and a forward biased rectifying junction.

11. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems as in Claim 5, in which the semiconductor is silicon and at least one of the drain junctions comprises at least one material which forms a barrier height of approximately half the band-gap of the semiconductor with said semiconductor.

12. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems as in Claim 7, in which the semiconductor is silicon and at least one of the drain junctions comprises at least one material which forms a barrier height of approximately half the band-gap of the semiconductor with said semiconductor.

13. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems as in Claim 5, which further comprises a voltage bias source connected

across said electrically noninterconncted essentially non-rectifying source junctions so that they are held at different voltages, each voltage being selected from the group consisting of:

+V;
-V; and
Ground;

said voltage bias source providing a selection from the group consisting of:

having contact to the back of said substrate; and

not having contact to the back of said substrate.

14. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems as in Claim 7, which further comprises a voltage bias source connected across said electrically noninterconncted essentially non-rectifying source junctions so that they are held at different voltages, each voltage being selected from the group consisting of:

+V;
-V; and
Ground;

said voltage bias source providing a selection from the group consisting of:

having contact to the back of said substrate; and

not having contact to the back of said substrate.

15. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems as in Claim 5, in which at least one source or drain junction is characterized by at least one selection from the group consisting of:

being formed in a region etched into the semiconductor,

being formed by a process comprising vacuum deposition of said at least one material onto said semiconductor,

being formed by a process comprising diffusion of said at least one material into semiconductor,

being formed by a process comprising ion-implantation of said at least one material into said semiconductor, and

being comprised of said at least one material which forms a barrier height of approximately half the band-gap of the semiconductor.

16. An inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complementary Metal Oxide Semiconductor (CMOS) systems as in Claim 7, in which at least one source or drain junction is characterized by at least one selection from the group consisting of:

being formed in a region etched into the semiconductor,

being formed by a process comprising vacuum deposition of said at least one material onto said semiconductor,

being formed by a process comprising diffusion of said at least one material into said semiconductor,

being formed by a process comprising ion-implantation of said at least one material into said semiconductor, and

being comprised of said at least one material which forms a barrier height of approximately half the band-gap of the semiconductor.

17. An inverting single device with operating characteristics similar to dual device seriesed N and P-Channel MOSFETS CMOS systems comprising two oppositely facing electrically interconnected rectifying diodes in a semiconductor epi-layer or substrate characterized by a selection from the group consisting of:

said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and

said semiconductor contains both N and P-type

metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels;

wherein a forward direction of rectification of each of said electrically interconnected rectifying diodes changes depending upon what type, N or P, be it metallurgically or field induced, is present in the semiconductor, said inverting single device with operating characteristics similar to dual device seriesed N and P-Channel MOSFETS CMOS systems further comprising gate means for field inducing effective doping type in said semiconductor, said gate means being set off from said semiconductor by insulator and each of said electrically interconnected rectifying diodes having an electrically non-interconnected terminal; and wherein, in use, the electrically non-interconnected terminals of the oppositely facing rectifying diodes are held at different voltages, and a voltage between said applied different voltages, inclusive, is monitored at the electrical interconnection between said two oppositely facing rectifying diodes, which monitored voltage responds inversely to applied gate voltage, said monitored voltage being essentially electrically isolated from said gate voltage and appearing at said electrical interconnection between said two oppositely facing rectifying diodes primarily through the rectifying diode which is caused to be forward biased as a result of semiconductor type metallurgically present or field induced by said applied gate voltage;

the basis of operation of said inverting single device with operating characteristics similar to dual device seriesed N and P-Channel MOSFETS CMOS systems being that said two oppositely facing electrically interconnected rectifying diodes are each comprised of at least one material that forms a rectifying junction to semiconductor when it is either N or P-type by either

metallurigical or field induced means, and the presence of at least partially compensated semiconductor which comprises both N and P-type carriers enables easy provision of N and P-type channel region forming carriers via gate voltage application effected field effect means.

18. An inverting single device as in Claim 17, in which the semiconductor further comprises at least one region of parasitic current flow blocking material which prevents parasitic currents from flowing to or away therefrom through said at least one region of parasitic current flow blocking material, said at least one region of parasitic current flow blocking material being present at at least one selection from the group consisting of:

physically a part of the inverting single device comprising an extention of the electrical interconnection between the two oppositely facing electrically interconnected rectifying diodes; and

physically separate from the inverting single device;

said at least one region of parasitic current flow blocking material forming rectifying junctions with both N and P-type metallurgical or field induced semiconductor.

19. An inverting single device as in Claim 17, in which the semiconductor is silicon and the two oppositely facing electrically interconnected rectifying diodes comprise at least one material that forms a barrier height of approximately half the band-gap thereof with said silicon.

20. An inverting single device as in Claim 17, which further comprises a voltage bias source connected across said electrically noninterconncted terminals of the oppositely facing

rectifying diodes so that they are held at different voltages, each voltage being selected from the group consisting of:

+V;
-V; and
Ground.

21. An inverting single device as in Claim 17, in which at least one said electrically interconnected rectifying diode comprising rectifying junction is characterized by at least one selection from the group consisting of:

being formed in a region etched into the semiconductor,

being formed by a process comprising vacuum deposition of said at least one material onto said semiconductor,

being formed by a process comprising diffusion of said at least one material into said semiconductor,

being formed by a process comprising ion-implantation of said at least one material into said semiconductor, and

being comprised of said at least one material which forms a barrier height of approximately half the band-gap of the semiconductor.

22. A semiconductor system as in Claim 1 in which the semiconductor region is characterized as being at least one selection from the group consisting of:

single crystal;
amorphous;
intermediate to single crystal and amorphous.

23. A semiconductor system as in Claim 2 in which the semiconductor region is characterized as being at least one selection from the group consisting of:

single crystal;
amorphous;
intermediate to single crystal and amorphous.

24. A semiconductor system as in Claim 3 in which the semiconductor region is characterized as being at least one selection from the group consisting of:

single crystal;
amorphous;
intermediate to single crystal and amorphous.

25. A semiconductor system as in Claim 5 in which the semiconductor epi-layer or substrate is characterized as being at least one selection from the group consisting of:

single crystal;
amorphous;
intermediate to single crystal and amorphous.

26. A semiconductor system as in Claim 7 in which the

semiconductor epi-layer or substrate is characterized as being at least one selection from the group consisting of:

single crystal;
amorphous;
intermediate to single crystal and amorphous.

semiconductor epi-layer or substrate

27. A semiconductor system as in Claim 17 in which the semiconductor epi-layer or substrate is characterized as being at least one selection from the group consisting of:

single crystal;
amorphous;
intermediate to single crystal and amorphous.